AMENDMENTS TO THE SPECIFICATION

In the specification

Please replace paragraph [0001] with the following amended paragraph:

[0001] The present invention relates to an ~~active driver for~~ internal voltage generating circuit ~~an internal voltage~~ and, more specifically, to an ~~active driver~~ internal voltage generating circuit that can minimize an increase of active consumption current depending on the size of a transistor for a driver used in an active operation.

Please replace [0003] with the following amended paragraph:

[0003] Generally, variation in a load of peripheral circuits, memory arrays, etc., which receive an internal voltage (VINT), is very severe within a DRAM. It is thus difficult to design a circuit having a stabilized operation. For example, an internal voltage (VINT) that is used in a DRAM core, i.e., on the side of a cell and a sub word line driver, a sense amplifier, a X-decoder and a Y-decoder includes a core voltage (VCORE) and a high voltage (VPP) being an electrostatic potential voltage. For instance, if the external power supply voltage (VDD) becomes 2.5V, a core voltage (VCORE) becomes 1.8V. If the external power supply voltage (VDD) is 2.5V, the high voltage (VPP) becomes 3.5V to 3.9V. In an active operation of a DRAM, the core voltage (VCORE) is used. A large amount of current is consumed accordingly. Therefore, the core voltage (VCORE) is generated by an ~~active driver for~~ internal voltage generating ~~an internal voltage~~ circuit using an operational amplifier.

Please replace paragraph [0004] with the following amended paragraph:

[0004] Fig. 1 is a circuit diagram illustrating the configuration of a ~~full driver used as an active driver for generating an internal voltage in a related art~~ conventional internal voltage generating circuit;

Please replace paragraph [0005] with the following amended paragraph:

Referring to Fig. 1, a conventional ~~active driver for generating the internal voltage~~ internal voltage generating circuit receives a reference voltage (VREFC) of about

1.8V to output a core voltage (VCORE) of 1.8V. In general, the ~~active driver for generating the internal voltage~~ internal voltage generating circuit consists of an operational amplifier 16, an output driver 14 and an n-channel MOSFET 18 (hereinafter, referred to as 'NMOS transistor'). The operational amplifier 16 has a non-inverse input terminal (+) to which a reference voltage (VREFC) is inputted and an inverse input terminal (-) to which an output voltage (VCORE) is inputted, and provides the output signal to a gate electrode of a p-channel MOSFET (hereinafter, referred to as 'PMOS transistor') of the output driver 14. The output driver 14 has a source electrode to which an external power supply voltage (VDD) is inputted and a drain electrode connected to an output terminal 20. The NMOS transistor 18 is operated by a control voltage (VCON; 0.8V), so that the potential of the output terminal 20 becomes a ground voltage (VSS). As a result, a core voltage (VCORE) that is dropped from the external power supply voltage (VDD) is outputted from the NMOS transistor 18.

Please replace paragraph [0006] with the following amended paragraph:

[0006] This ~~active driver for generating the internal voltage~~ internal voltage generating circuit further includes a PMOS transistor 12 having a gate electrode to which an active signal (act) is inputted so that the driver operates only in an active operation. The PMOS transistor 12 has a source electrode to which the external power supply voltage (VDD) is inputted, and a drain electrode connected to the drive node 19. The PMOS transistor 12 is operated by the active signal (act). If the active signal (act) that is activated in an active operation is inputted as a Low state, the PMOS transistor 12 is turned on and the drive node 19 becomes a High state due to the external power supply voltage (VDD). The output driver 14 is thus turned off. Meanwhile, if the active signal (act) is shifted from a Low state to a High state, that is, when the DRAM is in an active operation, the output driver 14 is turned on.

Please replace paragraph [0008] with the following amended paragraph:

As described above, there is a limit in increasing the size of the output driver 14. For example, a level of the core voltage (VCORE) drops by current consumed in an active operation. After a given delay by a response speed of the ~~active driver for generating the internal voltage~~ internal voltage generating circuit, the PMOS transistor of the output

driver 14 is operated. Thereafter, the level of the core voltage (VCORE) that drops by the operation of the PMOS transistor of the output driver 14 is forcibly boosted. At this time, if the size of the PMOS transistor of the output driver is large, it is over-damped higher than the core voltage (VCORE) level. Thus, lots of time is consumed until the voltage of the PMOS transistor is restored to an original core voltage (VCORE) level. Furthermore, if the size of the PMOS transistor of the output driver 14 is increased, a layout area of a circuit is also increased.

Please replace paragraph [0012] with the following amended paragraph:

In addition, the present invention is directed to minimizing an increase of a total layout area occupied by an internal voltage ~~active driver~~ generating circuit, by minimizing an increase in the size of a PMOS transistor of an output driver in the internal voltage ~~active driver~~ generating circuit using the PMOS transistor.

Please replace paragraph [0013] with the following amended paragraph:

According to a preferred embodiment of the present invention, there is provided an ~~active driver~~ internal voltage generating circuit, including an internal voltage-generating unit for converting an external power supply voltage into an internal voltage according to a reference voltage and outputting, and at least one internal voltage drop control unit that is operated by an enable signal generated by detecting a voltage level of the internal voltage, for stabilizing the internal voltage to a constant voltage level.

Please replace paragraph [0014] with the following amended paragraph:

[0014] Fig. 1 is a circuit diagram illustrating the configuration of an ~~active driver for generating an~~ internal voltage generating circuit in a related art;

Please replace paragraph [0015] with the following amended paragraph:

[0015] Fig. 2 is a circuit diagram illustrating the configuration of an ~~active driver for generating an~~ internal voltage generating circuit according to a preferred embodiment of the present invention;

Please replace paragraph [0018] with the following amended paragraph:

[0018] Fig. 5 is a waveform shown to explain the operation of the ~~active driver for generating the~~ internal voltage generating circuit shown in Fig. 2;

Please replace paragraph [0022] with the following amended paragraph:

[0022] Fig. 2 is a circuit diagram illustrating the configuration of an ~~active driver for generating an~~ internal voltage generating circuit according to a preferred embodiment of the present invention. It should be noted, however, that the ~~active driver for generating the~~ internal voltage generating circuit according to the present invention is not limited to a full driver and a half driver can be used instead.

Please replace paragraph [0023] with the following amended paragraph:

Referring to Fig. 2, the ~~active driver for generating the~~ internal voltage generating circuit includes an internal voltage-generating unit 100 and an internal voltage drop control unit 130. The internal voltage-generating unit 100 has an operational amplifier 116 and an output driver 114, for converting an external power supply voltage (VDD) into an internal voltage according to a reference voltage (VREFC). The internal voltage-generating unit 100 further includes a ground control unit 118 for connecting the output terminal 120 to the ground voltage (VSS) and a device having a resistor, and an active operation unit 112.

Please replace paragraph [0032] with the following amended paragraph:

[0032] It is preferable that the active operation unit 112 consists of a PMOS transistor in order to control the operation of the ~~active driver for generating the~~ internal voltage generating circuit so that the ~~active driver~~ circuit operates only in an active operation. In this case, the PMOS transistor is driven by the active signal (act) to transfer the power supply voltage (VDD) to the drive node 119. For example, the active operation unit 112 may consist of a switching device such as an NMOS transistor in place of a PMOS transistor. In its operation, if the active signal (act) is inputted as a Low state, the PMOS transistor is turned on and the external power supply voltage (VDD) is accordingly supplied to the drive

node 119. The PMOS transistor of the output driver 114 is thus turned off. As a result, the ~~active driver for generating the~~ internal voltage generating circuit does not operate.

Please replace paragraph [0042] with the following amended paragraph:

[0042] Operation examples of the ~~active driver for generating the~~ internal voltage generating circuit according to preferred embodiments of the present invention will now be described with reference to Operation Example 1 and Operation Example 2 shown in Fig. 5. Fig. 6 is a graph indicating a simulation result of Operation Example 1 shown in Fig. 5, and Fig. 7 is a graph indicating a simulation result of Operation Example 2 shown in Fig. 5.

Please replace paragraph [0052] with the following amended paragraph:

[0052] Meanwhile, in the present embodiments, the total size of all the PMOS transistors used as a driver is set to 100 and this size is distributed to respective PMOS transistors. That is, in a prior art, a single PMOS transistor is used for a driver. Thus, the size of the conventional PMOS transistor for the driver corresponds to the total size of a number of PMOS transistors for the driver according to an embodiment of the present invention. Accordingly, in a related art, a PMOS transistor for a driver operates unconditionally without regard to a voltage level of a core voltage (VCORE) in an active operation. In the internal voltage ~~active driver~~ generating circuit according to the present invention, however, as a corresponding PMOS transistor for a driver is variably operated in accordance with the voltage level of the core voltage (VCORE), an over-damping condition and an operating consumption current can be reduced compared to a prior art.

Please replace paragraph [0055] with the following amended paragraph:

[0055] In addition, according to the present invention, in an internal voltage ~~active driver~~ generating circuit using a PMOS transistor of an output driver, an increase in the size of a PMOS transistor of an output driver is minimized. Therefore, a total layout area occupied by an internal voltage ~~active driver~~ generating circuit can be minimized.